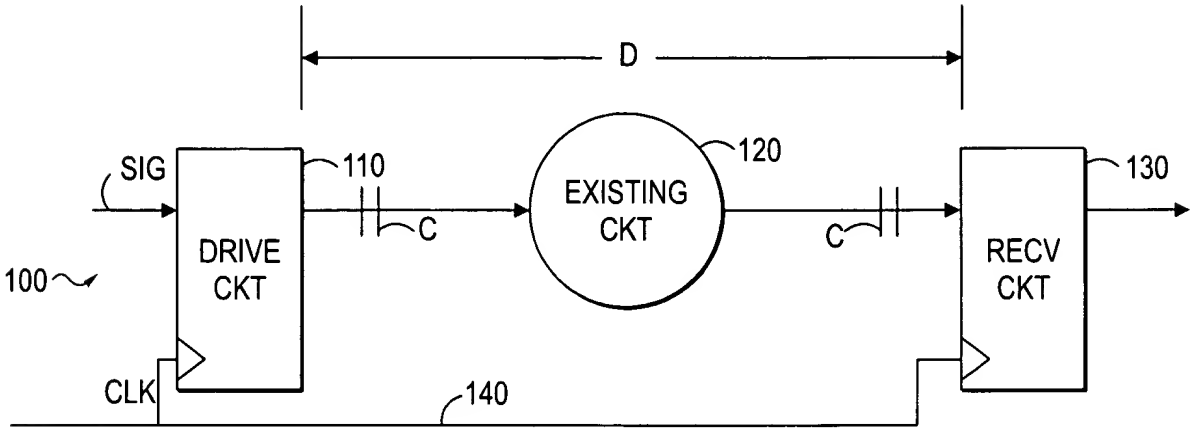


FIG. 1

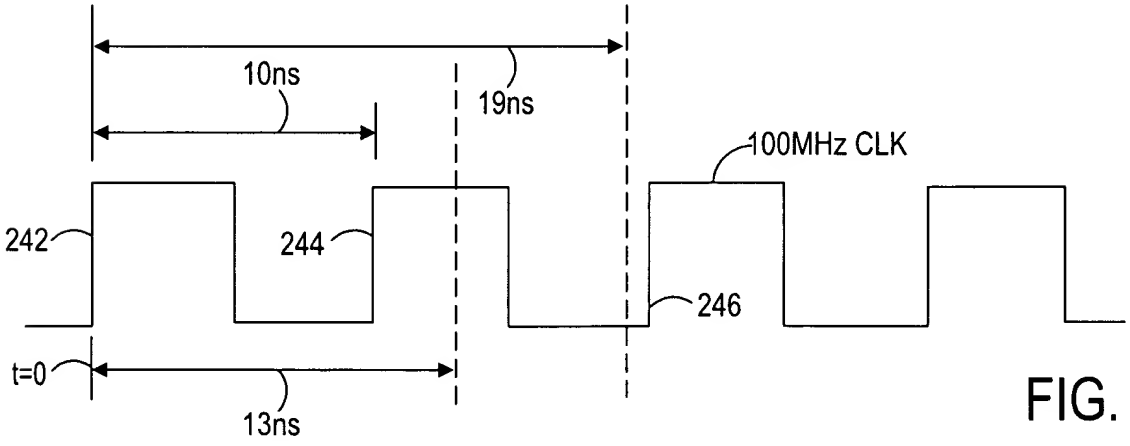


FIG. 2

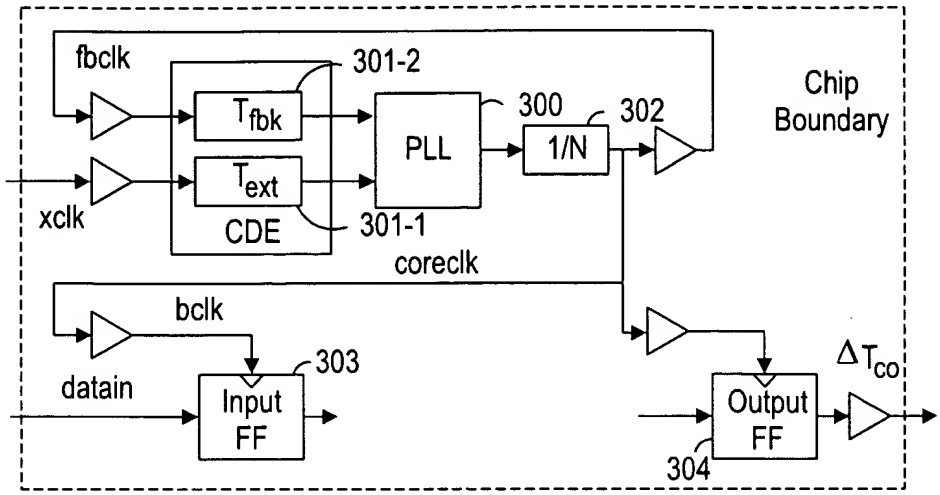


FIG. 3

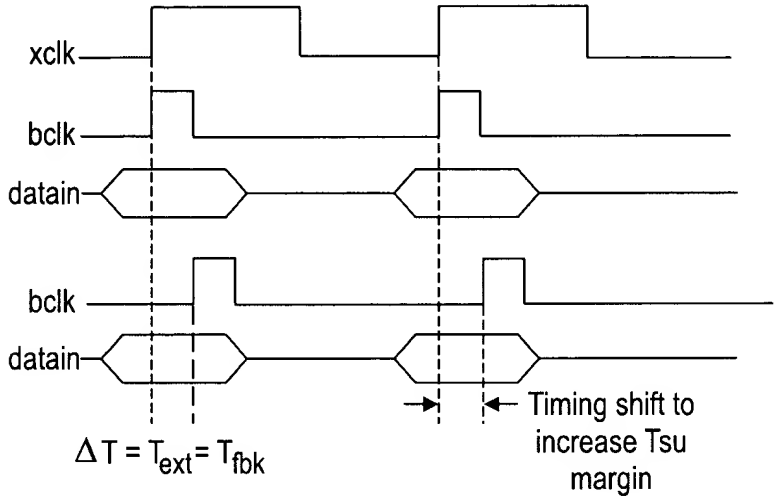


FIG. 4

Fix	Margin On	Action	Add ΔT_{co}
Tsu	Too,max,Th	π_{ext}	-
Th	Too,min,Tsu	π_{fbk}	-
Th	-	π_{fbk}	Yes
Tco,max	Tsu	π_{fbk}	-
Tco,min	Th	π_{ext}	-
Tco,min	-	π_{ext}	Yes

FIG. 5

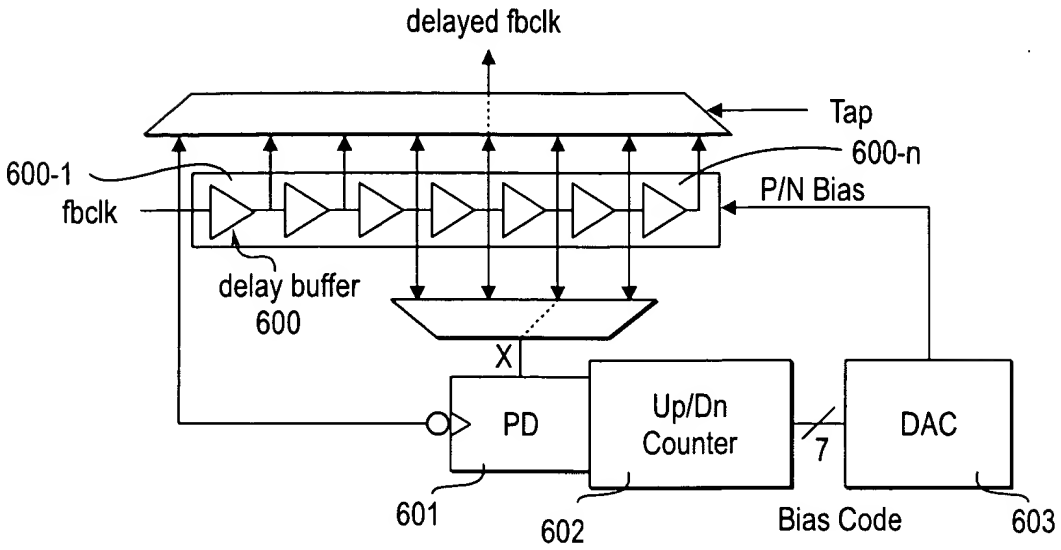

delayed fbclk
Tap
600-n
600-1
fbclk
P/N Bias
delay buffer
600
X
PD
Up/Dn
Counter
7
DAC
601
602
Bias Code
603

FIG. 6A

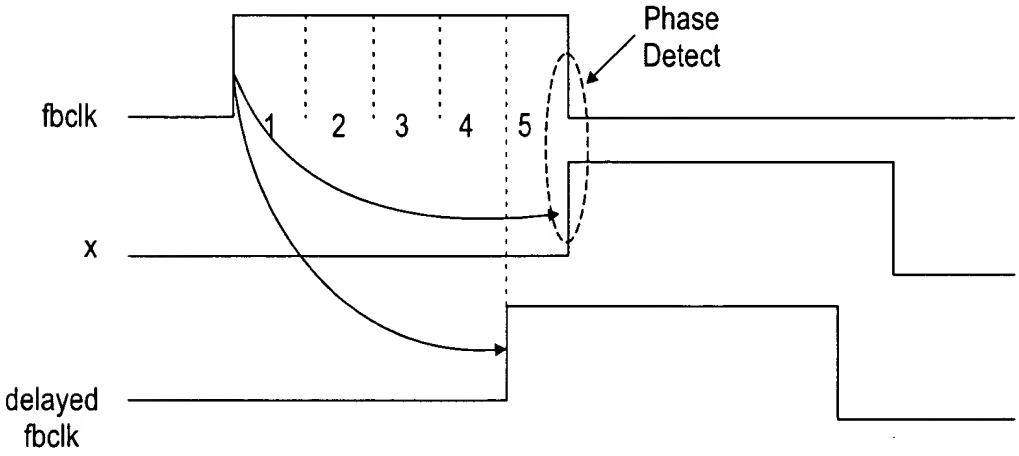

Phase
Detect
fbclk
1
2
3
4
5
x
delayed
fbclk

FIG. 6B

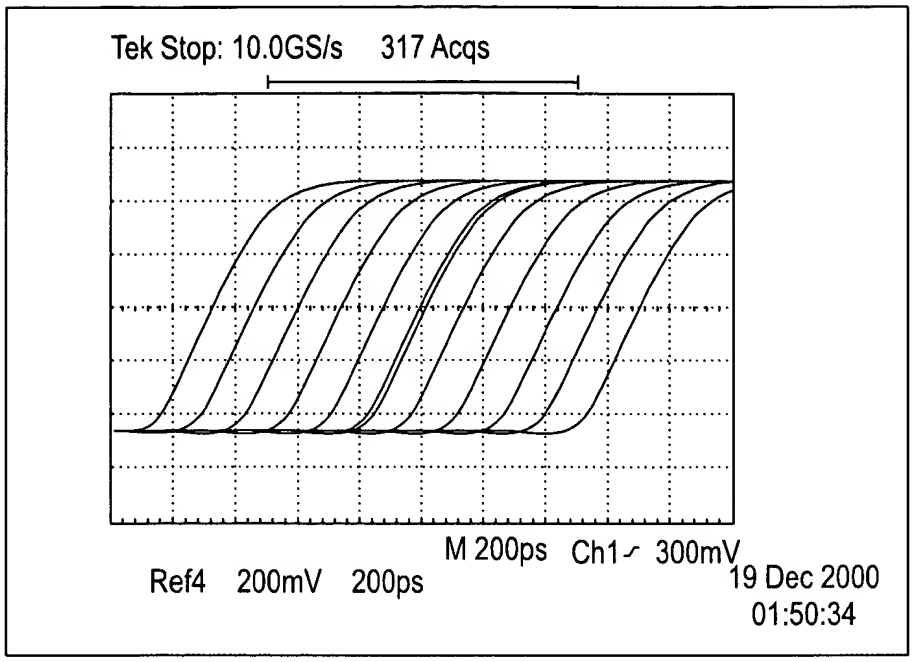

Tek Stop: 10.0GS/s 317 Acqs
M 200ps Ch1 300mV
Ref4 200mV 200ps
19 Dec 2000
01:50:34

FIG. 7

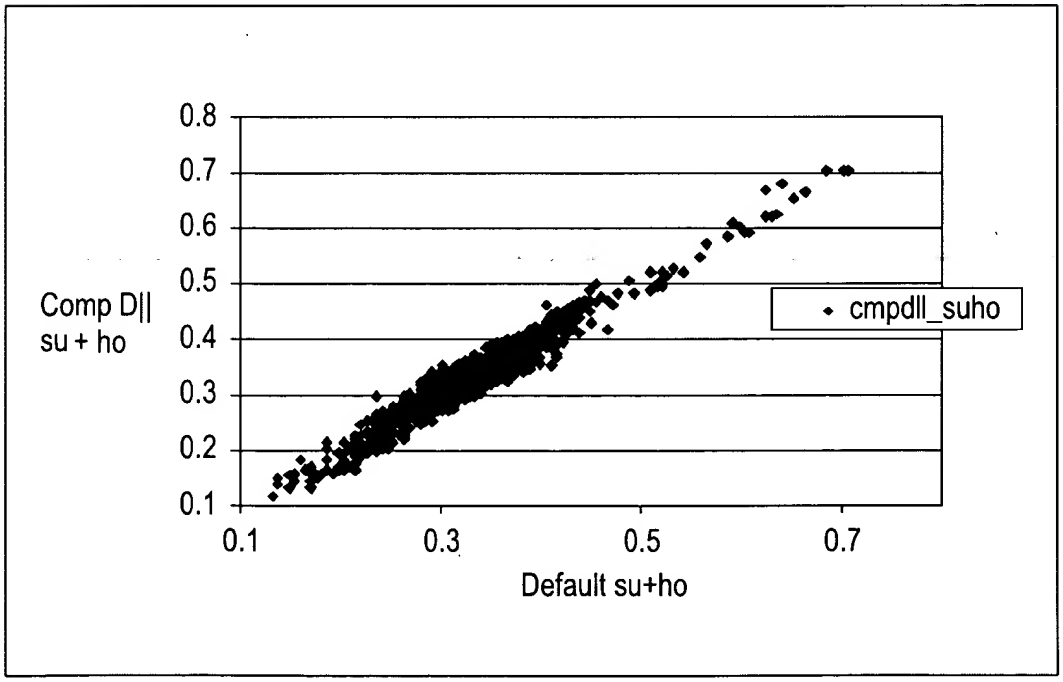

0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
Comp D||
su + ho
cmpdll_suho
0.1
0.3
0.5
0.7
Default su+ho

FIG. 8

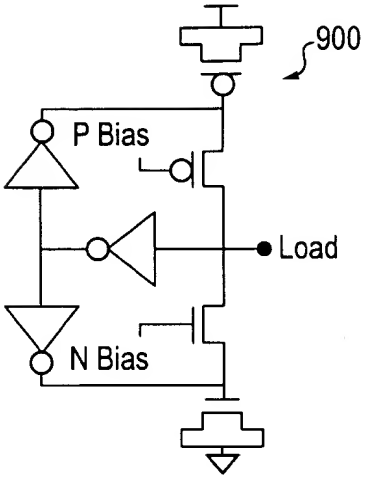


FIG. 9

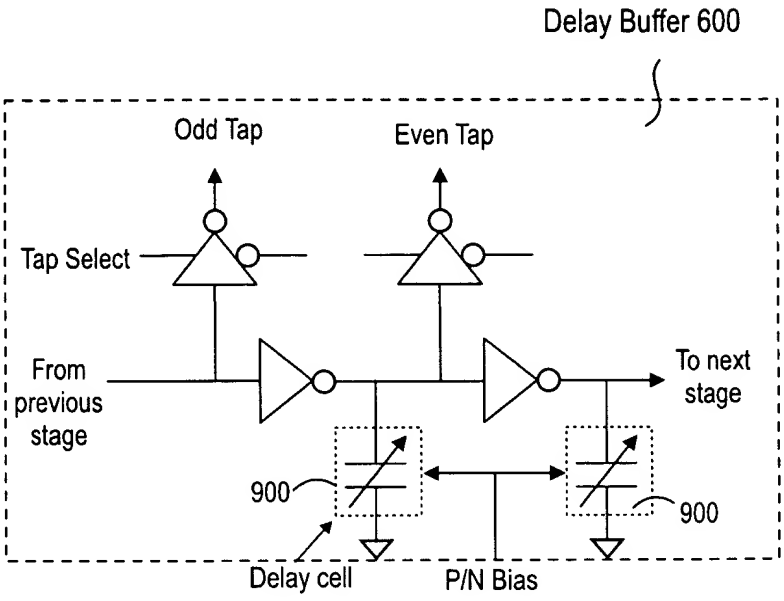


FIG. 10

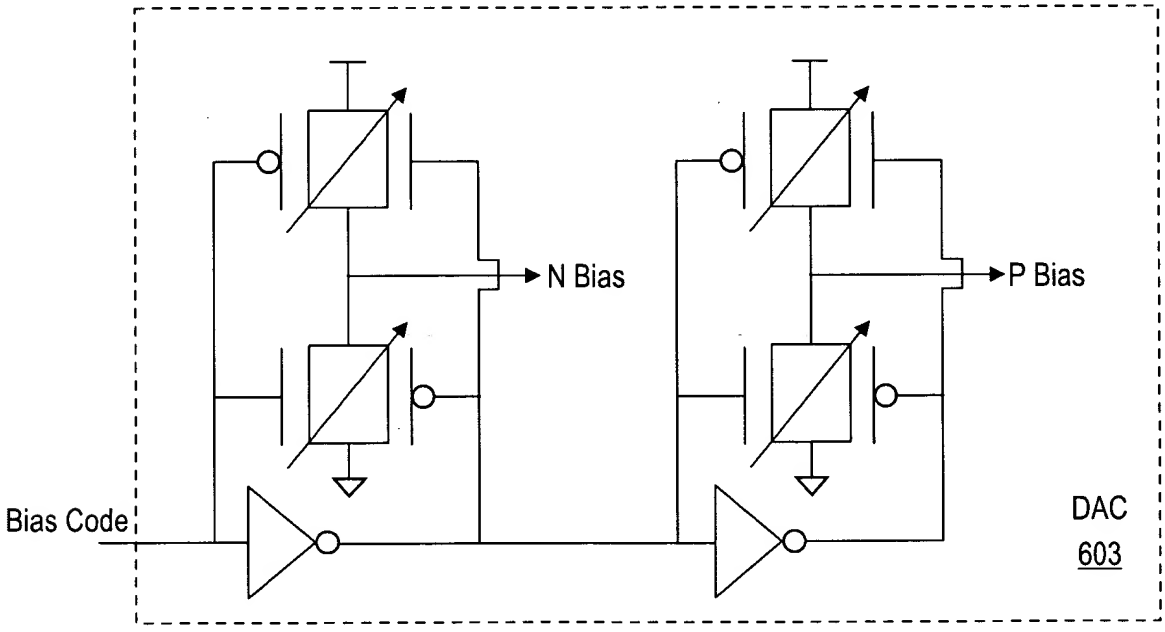
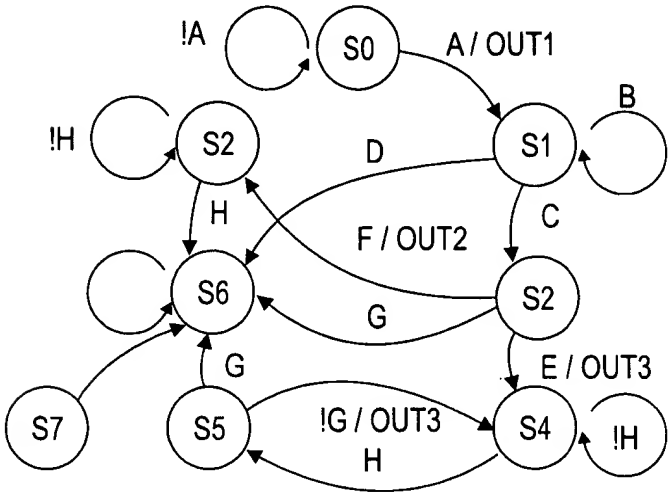


FIG. 11



Ⓐ	: Pwrgd
B	: (!CDElock·PLLlock) + !PLLlock
C	: CDElock·PLLlock-FSMen
D	: PLLlock·!FSMen
E	: !TapEqFuse·!Mlock
F	: !TapEqFuse·Mlock
G	: TapEqFuse
H	: PLLlock
OUT1	: if (FSMen), Tap = 000; Else Tap = Fuse Value
OUT2	: Tap = Fuse Value
OUT3	: Tap = Tap + 1

FIG. 12

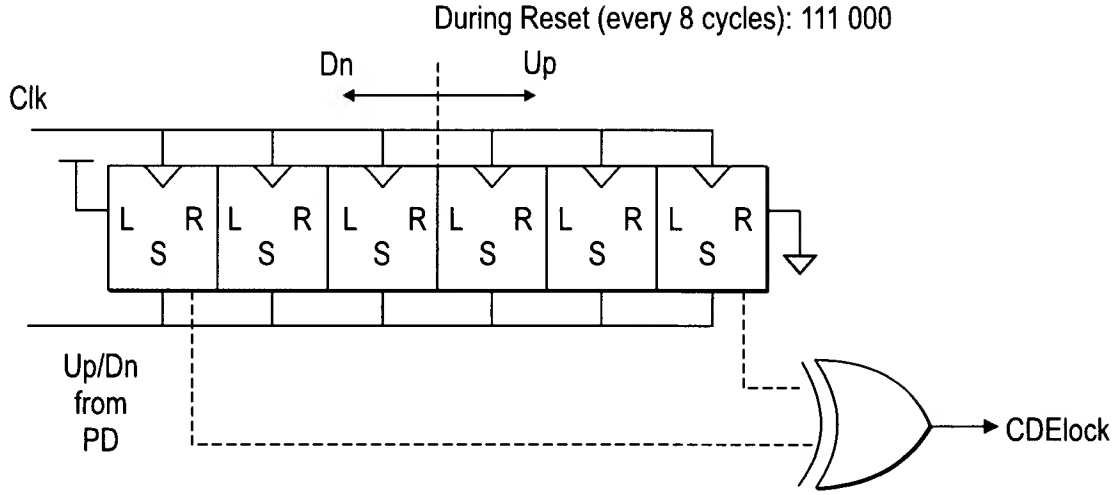

During Reset (every 8 cycles): 111 000
Dn
Up
Clk
L R
S
Up/Dn
from
PD
CDElock

FIG. 13

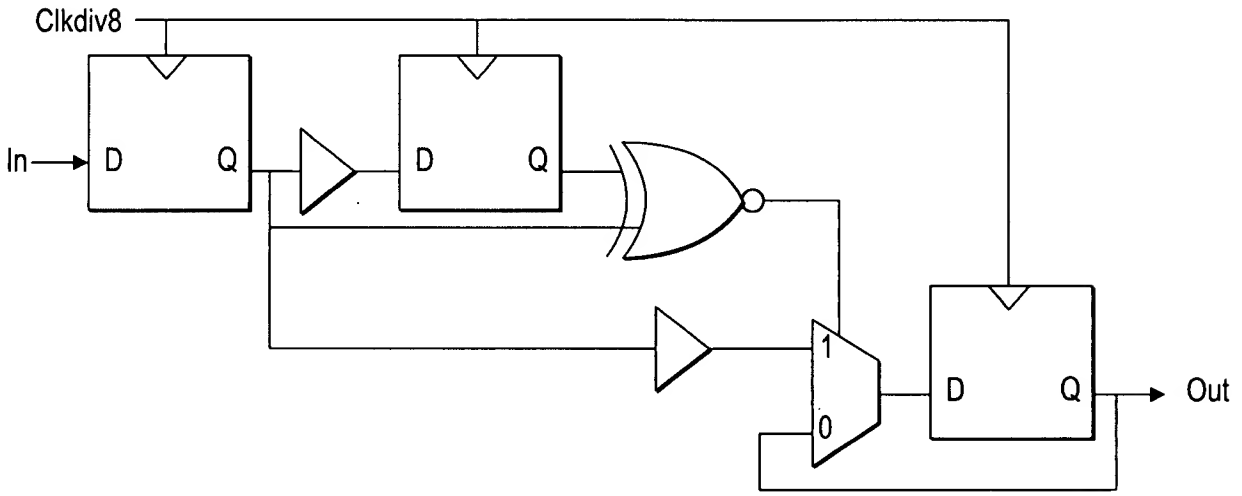

Clkdiv8
In
D
Q
1
0
Out

FIG. 14

Condition	Voltage	Bias Code
95nm,95°C	1.10V	1000101
(Slow)	1.25V	0110011
	1.40V	0101100

Condition	Voltage	Bias Code
75nm,5°C	1.10V	0101110
(Fast)	1.25V	0100101
	1.40V	0011101

FIG. 15

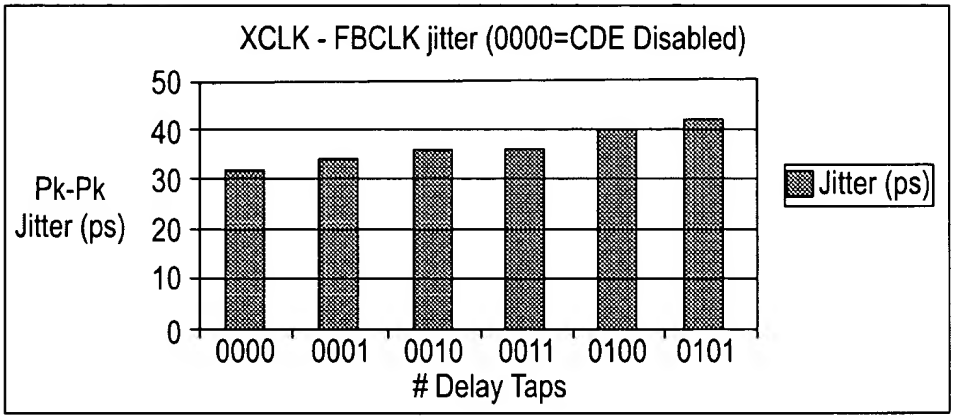


FIG. 16

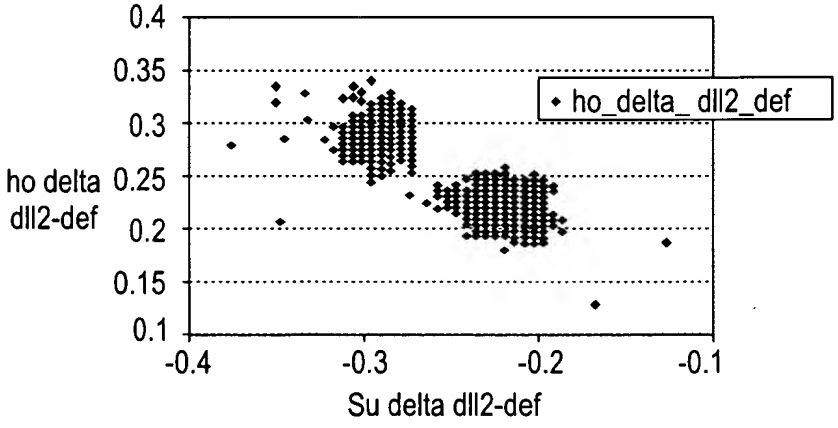


FIG. 17